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(72) Inventor NEVILLE DAVID KNEE

(54) IMPROVEMENTS IN OR RELATING TO METHODS OF FABRICATING INTEGRATED CIRCUITS

(72) We, GEC SEMICONDUCTORS LIMITED, of East Lane, Wembley, Middlesex HA9 7PP, a British Company, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to methods of fabricating integrated circuits.

In the fabrication of an integrated circuit it is common practice to provide the semiconductor material in which the circuit is to be formed with a member of electrically insulating material which serves as a mechanical support for the semiconductor material. The support member normally extends into channels formed through the semiconductor material to divide the semiconductor material into an array of islands, the support member material thus serving to isolate the islands physically and electrically in addition to providing a mechanical support for the semiconductor material. The support member material is typically polycrystalline silicon.

In such processes it is important to keep the main faces of the semiconductor material as flat as possible to facilitate the execution of etching and polishing operations carried out on the material. Unfortunately, the provision of a support member militates against this since the support member is normally formed at high temperature of a material having a different coefficient of thermal expansion from the semiconductor material with the result that the composite structure bows on cooling to room temperature.

It is an object of the present invention to provide a method of fabricating integrated circuits wherein this difficulty is alleviated.

According to the present invention in a method of fabricating an integrated circuit wherein semiconductor material in which the circuit is to be formed is provided with a member of electrically insulating material which serves as a mechanical support for the semiconductor material, said support member is formed as a laminated structure comprising layers of different material which, with changes in temperature, tend to bow the composite structure in opposite directions, the relative thicknesses of the layers of the laminated structure being such as to minimise the bowing of the composite structure.

In one particular method in accordance with the invention said support member is formed as alternate layers of polycrystalline silicon and silicon oxide.

One method in accordance with the invention will now be described by way of example with reference to the drawings filed with the Provisional Specification in which Figures 1 to 6 are sectional diagrams illustrating various stages in the fabrication of an integrated circuit.

Referring to Figure 1, a thin epitaxial layer 1 of low resistivity N-type silicon is first formed in known manner on one main face of a monocrystalline wafer 2 of high resistivity N-type silicon, the wafer 2 having accurately parallel main faces. The external surface of the body thus formed is then provided with a silicon oxide layer 3 in known manner, as shown in Figure 2. Windows 4 are then opened in the part of the oxide layer 3 adjacent the epitaxial layer 1 using known photolithographic and etching processes, and by further etching in known manenr through the windows 4, channels 5 extending through the epitaxial layer 1 into the underlying wafer 2 are formed, as shown in Figure 3.

The remaining parts of the silicon oxide layer 3 on the epitaxial layer 1 are then etched off in known manner and a new silicon oxide layer 6 is formed on the exposed surface of the epitaxial layer 1 and in the channels 5, as shown in Figure 4.

A laminated structure comprising alternate

thermally grown layers 7 and 8 consisting of polycrystalline silicon and silicon oxide respectively is then formed on the silicon oxide layer 6 to provide a dielectric support member 9 for the semiconductor material comprising the wafer 2 and the channelled epitaxial layer 1, the layers 7 and 8 extending into the channels as shown in Figure 5.

Due to the different coefficients of thermal expansion of the materials involved, the polycrystalline silicon layers 7 tend on cooling to bow the composite structure in one direction whilst the silicon oxide layers 8 tend on cooling to bow the composite structure in the opopsite direction.

By careful control of the relative thicknesses of the polycrystalline silicon and silicon oxide layers 7 and 8 overall bowing of the composite structure is reduced to a minimum. The overall thickness of the support member 9 is made sufficient to prevent breakage of the composite structure during subsequent fabrication stages.

After formation of the support member 9 the face of the composite structure remote from the support member 9 is lapped and polished until the parts of the support member 9 in the channels 5 are exposed, as shown in Figure 6. The semiconductor material comprising the remainder of wafer 2 and the channelled epitaxial layer 1 is thus divided into semiconductor islands which are isolated physically and electrically by the parts of the support member 9 in the channels 5.

In subsequent stages of the process (not illustrated) the required integrated circuit components are formed in the isolated semiconductor islands and electrical interconnections between these components are formed using techniques well known in the integrated circuit art.

In one particular method as described above by way of example the polycrystalline silicon layers 7 have a thickness of 15 microns and the silicon oxide layers 8 have a thickness of 0.3 micron. The polycrystalline silicon layers 7 are conveniently formed by thermal deposition from a stream of trichlorosilene vapour containing hydrogen as a reducing gas, and the silicon oxide layers 8 are conveniently formed by introducing carbon dioxide into the trichlorosilene/hydrogen gas stream. The deposition is suitably carried out at a temperature of 1050° C under conditions such that the growth rate of polycrystalline silicon is 3 microns per minute and the growth rate of silicon oxide is 0.06 micron per minute. It will be apprecilated that care must be taken to establish a uniform temperature over the structure during thermal deposition.

In addition to minimising bowing the method according to the invention exhibits further advantages over known methods in which the support member consists solely of polycrystalline silicon. One such further advantage arises because a laminated polycrystalline silicon/silicon oxide support member has a greater rupture modulus and flexibility than a polycrystalline silicon support member. Hence, a laminated support member may be thinner than a support member consisting solely of polycrystalline silicon improving the thermal properties of the composite structure and reducing processing time. Another advantage is that the alternate polycrystalline silicon and silicon layers act as a number of capacitors connected in series between the semiconductor islands and the face of the composite structure remote from the islands, thus reducing the capacitance between the islands and this face of the structure to which a metal header is normally bonded.

It will be appreciated that whilst polycrystalline silicon and silicon oxide are used for the support member in the method described above by way of example, other materials may be used, for example polycrystalline silicon and silicon carbide.

Furthermore the invention is applicable to methods of fabricating integrated circuits other than the particular method described above. For example the invention can be applied to the so-called "etch out and backfill" fabrication process described in the following articles

(a) "The minimisation of parasitics in integrated circuits by dielectric isolation" by D. A. Maxwell, R. H. Beeson and D. F. Allison, pages 20 to 25 of the January 1965 edition of IEEE Transactions, Electron Devices.

(b) "Dielectric isolated integrated circuit substrate processing" by U. S. Davidsohn and F. Lee, pages 1532 and 1537 of the September 1969 issue of The Proceedings of the IEEE (Volume 57, number 9).

WHAT WE CLAIM IS:—

1. A method of fabricating an integrated circuit wherein semiconductor material in which the circuit is to be formed is provided with a member of electrically insulating material which serves as a mechanical support for the semiconductor material, said support member being formed as a laminated structure comprising layers of different materials which, with changes in temperature tend to bow the composite structure in opposite directions, the relative thicknesses of the layers of the laminated structure being such as to minimise the bowing of the composite structure.

2. A method according to Claim 1 wherein the support member extends into channels which extend through the semi-

conductor material so as to divide the semiconductor material into an array of islands.

3. A method according to Claim 1 or Claim 2 wherein said support member is formed as alternate layers of polycrystalline silicon and silicon oxide.

4. A method according to Claim 3 wherein the polycrystalline silicon layers are formed by thermal deposition from a stream of trichlorosilene vapour containing hydrogen as a reducing gas and the silicon oxide layers are formed by introducing carbon dioxide into the trichlorosilene/hydrogen gas stream.

5. A method of fabricating an integrated circuit substantially as hereinbefore described with reference to the drawing filed with the Provisional Specification.

6. An integrated circuit manufactured by a method according to any one of the preceding Claims.

For the Applicants,
M. B. W. POPE,
Chartered Patent Agent.

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1436434 PROVISIONAL SPECIFICATION
1 SHEET *This drawing is a reproduction of the Original on a reduced scale*

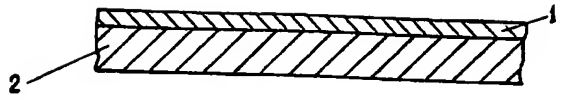

FIG.1.

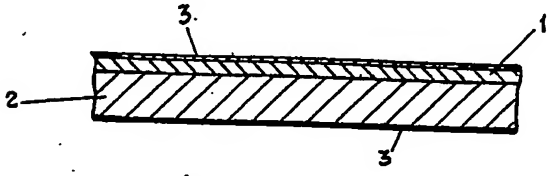

FIG.2.

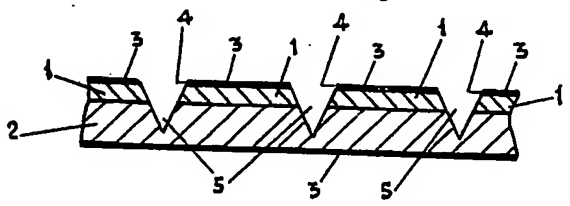

FIG.3.

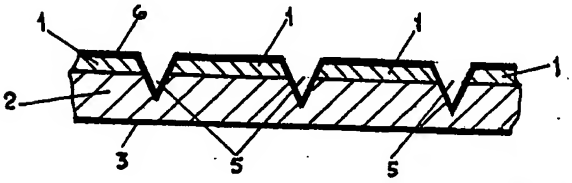

FIG.4.

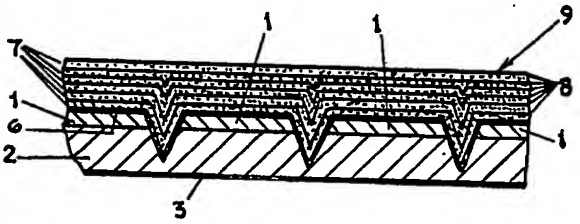

FIG.5.

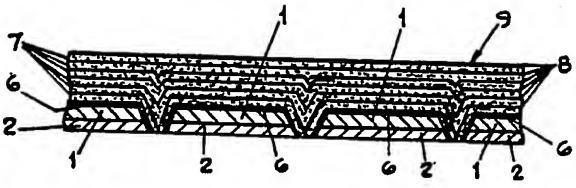

FIG.6.